WHAT IS CLAIMED IS:

1. A data processing device, capable of decoding and executing instructions, comprising:

a cache memory where said instructions are held,

5 wherein said instructions each contain a spare field, and

wherein said cache memory holds information which is generated according to predecoding of instructions in a first corresponding area corresponding to said spare field.

2. The data processing device according to claim 1,

10 further comprising:

controlling means which controls an executing sequence of said instructions based on information of said spare field, when executing instructions loaded from said cache memory.

15 3. The data processing device according to claim 2, further comprising:

a predecoder which predecodes said instructions to generate said information before instructions are stored into said cache memory.

20 4. The data processing device according to claim 3, wherein said predecoder decodes operation codes contained in first fields of said instructions.

5. The data processing device according to claim 4,

wherein information on a type of instruction obtained from decoding results from said predecoder is held in said first corresponding area of said cache memory.

6. The data processing device according to claim 5, wherein said type of instruction includes an information of whether said instruction is a branch instruction or not.

7. The data processing device according to claim 6, wherein said controlling means commands fetching an instruction of a branched place, when it determines that said instruction is a branch instruction according to said information in said first corresponding area of said cache memory.

8. The data processing device according to claim 7, further comprising:

a queuing buffer temporarily storing instructions loaded from said instruction cache memory; and

a target buffer which holds an address of said branched place, said instruction of said branched place, and a following address of said address of said branched place,

wherein said controlling means divides one branch operation into a prepare target instruction and a branch procedure instruction,

wherein said prepare target instruction commands the calculations of said address of said branched place and fetching of said instruction of said branched place,

wherein said branch procedure instruction commands
branch condition checks and branch procedures.

9. The data processing device according to claim 8,

wherein said controlling means issues commands to load said instruction of said branched place and said following address from said target buffer when said controlling means determines that said instruction is a branch procedure instruction according to said information of said queuing buffer which was loaded from first corresponding area of said cache memory.

10. The data processing device according to claim 3, further comprising:

a processor performing calculations using information contained in first fields of said instructions before storing said instructions in said cache memory.

11. The data processing device according to claim 10,

wherein based on said decoding results, said cache memory holds calculation results from said processor in a second corresponding area of said instruction cache memory corresponding to said first fields.

12. The data processing device according to claim 10,

wherein to handle relative branch instructions of program counters with n bit displacements, said processor adds information of n lower bits of addresses of said program counters for displacements of said first fields in an adding operation, and

wherein added results by said processor are held in said second corresponding area of said cache memory, and

wherein carry information of said adding operation is held in said first corresponding area.

13. A data processing device, capable of decoding and executing instructions, comprising:

a cache memory where said instructions are held; and

a predecoder which performs predecoding of said instructions before said instructions are stored in said cache memory,

wherein said cache memory holds information generated by said predecoding of said instructions in an area which has a one to one relation with said instructions.

14. The data processing device according to claim 13, further comprising:

controlling means which controls an executing sequence of said instructions based on said information,

when executing instructions are loaded from said cache memory.

15. The data processing device according to claim 14, wherein said area is an area corresponding to a spare field of an instruction.

16. A data processing device, capable of decoding and executing instructions, comprising:

a cache memory; and

a predecoder,

wherein when an instruction is loaded, information generated from predecoding an instruction code of said instruction by said predecoder is written to a first area in said cache memory, and

wherein said first area corresponds to a spare field of said instruction code.

17. The data processing device according to claim 16, further comprising:

a bus interface unit controlling input and output of data,

wherein said instruction is loaded from an external memory through said bus interface circuit to said cache memory, and

wherein data from said bus interface unit to said cache memory flows through said predecoder for precoding.

18. The data processing device according to claim 17,

wherein when said data processing device executes instructions loaded from said cache memory, said information stored in said first area is used.

19. The data processing device according to claim 18,

wherein said information stored in said first area includes an information on branching.

20. The data processing device according to claim 19, further comprising:

a floating point operation unit; and

a data cache memory.